Application Note

NOVOSENSE

Design Guide for NSD7315-Q1

AN-15-0021

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NOVOSENSE

ABSTRACT

In automotive electronics, there are many high-current motor driver requirements, for example window driver, seat driver, mirror driver, thermal management system. Therefore, NOVOSENSE launched a high-current H-Bridge motor control driver, which integrates four N-channel low Rdson MOSFETs, current sense and regulation, configurable slew rate and various protection features, which can help customers achieve safe and reliable motor control. This application note mainly introduces the important features and application tips of NSD7315-Q1.

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1.Function Block

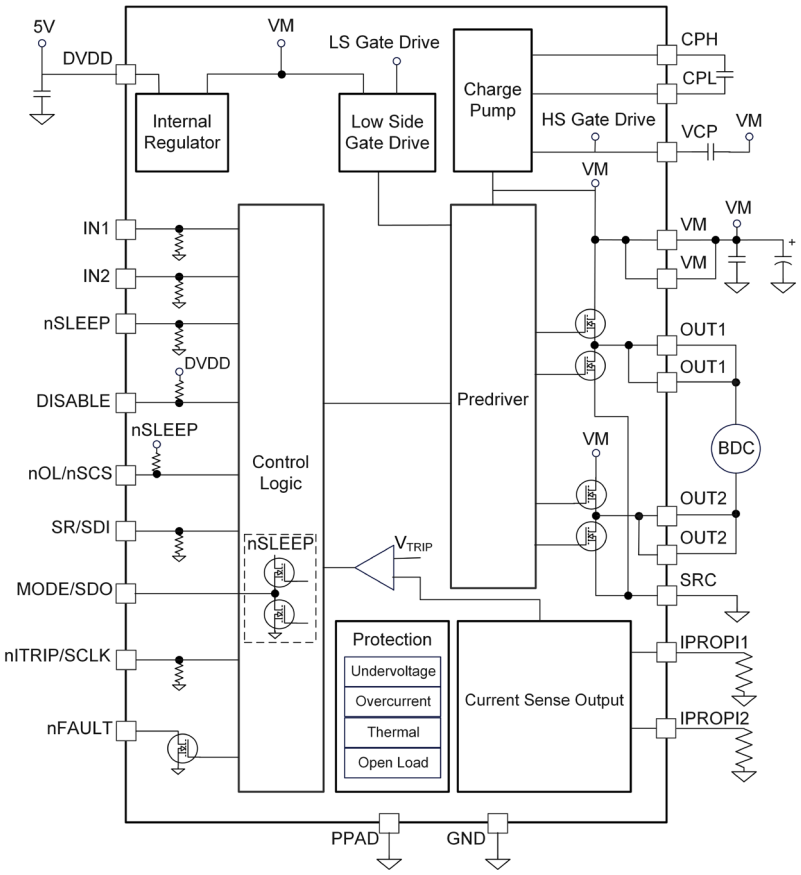


Figure 1.1 NSD7315-Q1 Block Diagram

- AEC-Q100 grade 1: –40°C to +125°C T_A
- SPI or Hardware interface options
- Rds(on) (High Side + Low Side): 150mΩ at T_J = 25°C, 13.5V
- Offer configurable control modes: PH/EN, PWM(IN1/IN2), Independent half-bridge control
- Integrated current sensing and regulation
- Configurable slew rate
- Protection Features:
  - UVLO: VM undervoltage lockout
  - CPUV: Charge pump undervoltage
  - OCP: Overcurrent protection
  - OL: Active and Passive open load detection
  - TSD: Thermal shutdown and thermal warning
  - Fault Condition output (nFAULT/SPI)

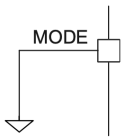
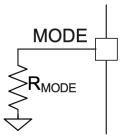
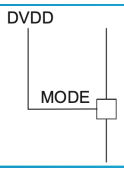
2.Control Modes

NSD7315-Q1 output has four N-channel MOSFETs configured in a H-bridge. The driver can be controlled using a PH/EN, PWM, or independent half-bridge input mode. Table 2.1 lists the control mode configurations. Table 2.2 lists the different MODE pin settings in hardware version.

Table 2.1 Control Mode Configuration

Hardware Device Mode Pin	SPI Device Mode Register	Control Mode
L	00b	PH/EN
H	01b(default)	PWM
200kΩ ± 5% to GND	10b	Independent half bridge
Not applicable	11b	Input disabled, bridge Hi-Z

Table 2.2 NSD7315H-Q1 Mode Pin Settings

Connection	Mode	Circuit
Connect to GND	PH/EN	
200kΩ ± 5% to GND	Independent half bridge	
Connect to DVDD	PWM	

In the hardware version of the device, the MODE pin latches on power-up or when exiting sleep mode. To change the mode settings, a power cycle or sleep reset must be performed on the device.

In the SPI version of the device, the mode setting can be changed by writing to the MODE register in the IC1 control register. The device mode gets latched when the DISABLE signal transitions from high to low. To change the mode settings, DISABLE pin should be high.

Table 2.3 EN/PH Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	FUNCTION
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	X	H	H	Brake (High Side Slow Decay)
1	0	1	0	L	H	Reverse (OUT2 -> OUT1)
1	0	1	1	H	L	Forward (OUT1 -> OUT2)
1	0	PWM	0	PWM	H	Reverse + High Side Decay
1	0	PWM	1	H	PWM	Forward + High Side Decay

Table 2.4 PWM Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	FUNCTION
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	0	Hi-Z	Hi-Z	Coast
1	0	0	1	L	H	Reverse (OUT2 -> OUT1)
1	0	1	0	H	L	Forward (OUT1 -> OUT2)
1	0	1	1	H	H	Brake (High Side Slow Decay)
1	0	PWM	1	PWM	H	Reverse + High Side Decay
1	0	1	PWM	H	PWM	Forward + High Side Decay

Table 2.5 Independent Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2	FUNCTION
0	X	X	X	Hi-Z	Hi-Z	Sleep
1	1	X	X	Hi-Z	Hi-Z	Disable
1	0	0	0	L	L	Brake (Low Side Slow Decay)
1	0	0	1	L	H	Reverse (OUT2 -> OUT1)
1	0	1	0	H	L	Forward (OUT1 -> OUT2)
1	0	1	1	H	H	Brake (High Side Slow Decay)
1	0	PWM	1	PWM	H	Reverse + High Side Decay
1	0	1	PWM	H	PWM	Forward + High Side Decay
1	0	PWM	0	PWM	L	Forward + Low Side Decay
1	0	0	PWM	L	PWM	Reverse + Low Side Decay

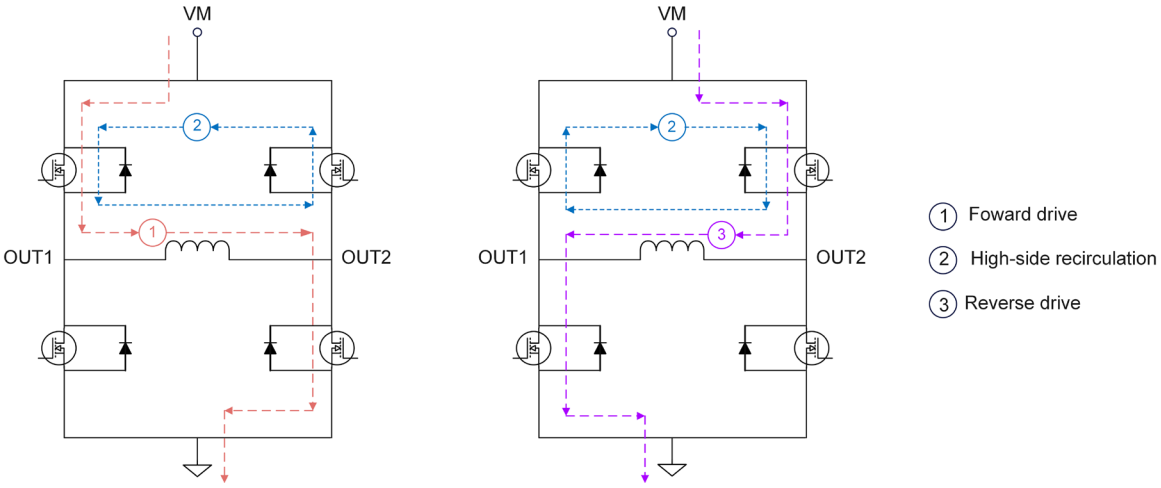


Figure 2.1 Forward/Reverse Drive and High Side Decay Path

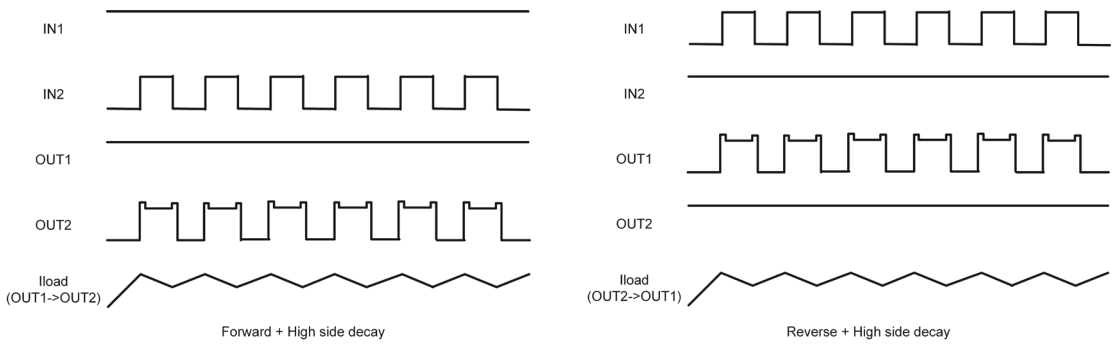


Figure 2.2 Forward/Reverse Drive and High Side Decay in PWM Mode

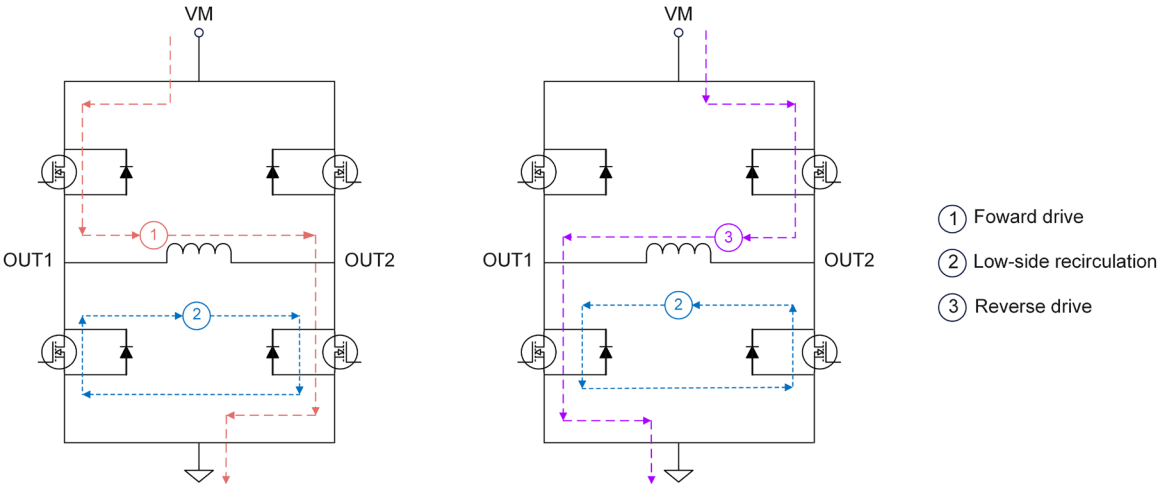


Figure 2.3 Forward/Reverse Drive and Low Side Decay Path

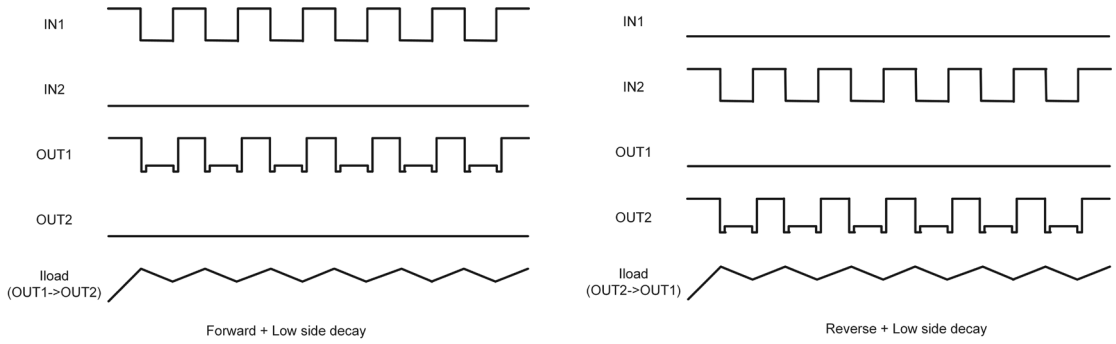


Figure 2.4 Forward/Reverse Drive and Low Side Decay in Independent Mode

3.Half-Bridge Mode

Depending on how the loads are connected on the outputs pin, some of the features offered by the device could have reduced functionality. For example, having a load between the OUTx and GND pins, as shown in Figure 3.1, results in false trips of the open-load diagnosis in active-mode (OLA). While having a load tied between the OUTx and VM pins restricts the use of internal current regulation because no means of measuring current flowing through the load with the current mirror block is available. Table 3.1 lists these use cases.

Table 3.1 Half-Bridge Mode Configuration

Load Connections		Functions	
Node1	**Node2**	**OLA**	**Current Regulation (I_{TRIP})**
OUTx	GND	Not Available	Operational
OUTx	VM	Operational	Not Available

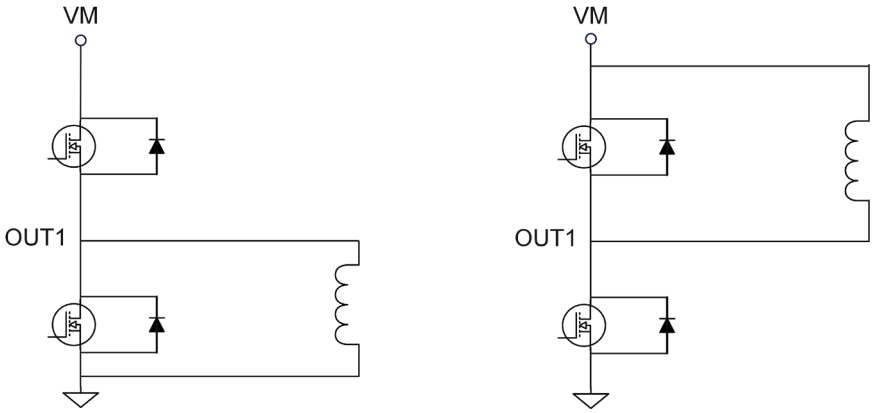


Figure 3.1 Independent Half-Bridge Mode Driving Low-side and High-side Loads

In the Independent half-bridge mode, OUT1_DIS or OUT2_DIS bit in the IC3 register can independently put the outputs of the half bridge in the high-impedance (Hi-Z) state. The option to independently set the outputs of the half bridge in the Hi-Z state is not available for the hardware version of the device.

And in the Independent half-bridge mode, the fault handling is performed independently for each half bridge. For example, if an overcurrent condition (OCP) is detected in half-bridge 1, only the half-bridge 1 output (OUT1) is disabled and half-bridge 2 continues to operate based on the IN2 input.

4.Current Sense

The IPROPI pin outputs an analog current that is proportional to the current flowing in the H-bridge. The output current is typically 1/1100 of the current in both high-side FETs. The IPROPI1 pin represents the current flowing through the HS1 MOSFET of half-bridge 1. The IPROPI2 pin represents the current flowing through the HS2 MOSFET of half-bridge 2.

To measure current with one sense resistor, the IPROPI1 and IPROPI2 pins must be connected together with the R_{SENSE} resistor. In this configuration, the current-sense output is proportional to the sum of the currents flowing through the both high-side FETs.

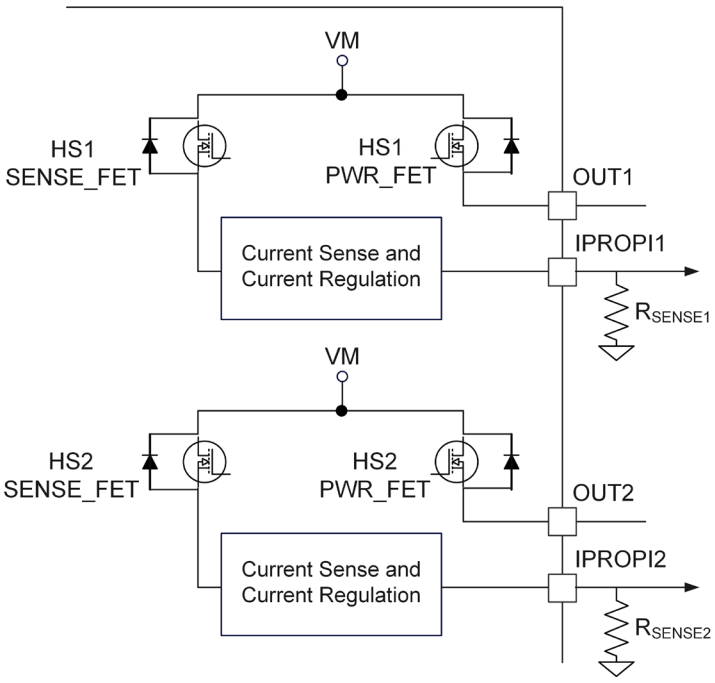


Figure 4.1 Current Sense Block Diagram

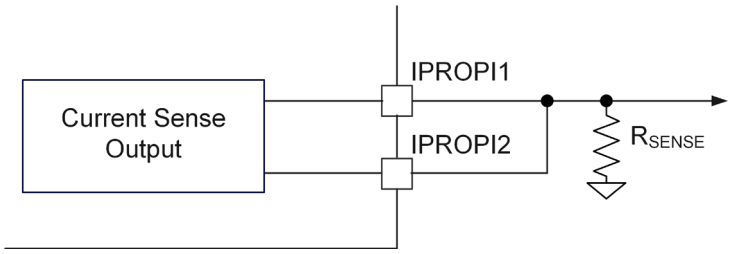


Figure 4.2 Current Sense with one sense resistor

The selection of the external resistor should be such that the voltage on the IPROPI pin is less than 5V. Therefore the resistor must be sized less than this value based on Equation 1. If the external resistor is selected too large cause IPROPI voltage higher than 5V, IPROPI pin will be clamped to 5V. And in this condition, current regulation function is disabled.

$$R_{SENSE}=k\times 5V/I_O \quad (1)$$

where

- K is the current mirror scaling factor, which is typically 1100.
- I_O is the maximum drive current to be monitored.

5.Current Regulation

When the ITRIP current has been reached and last for tDEG, the device enforces slow current decay by enabling both the high-side FETs for a time of t_{OFF}.

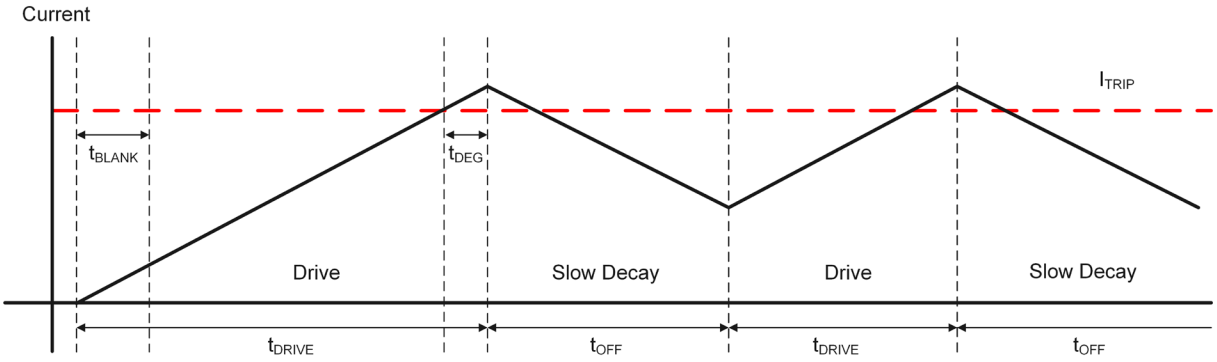


Figure 5.1 Current Regulation Time Period

The t_{OFF} time can't be interrupted when input changes state before t_{OFF} time ends, means that the device continues to decay until t_{OFF} ends. When the t_{OFF} time has elapsed and the current level falls below the current regulation I_{TRIP} level, the output is re-enabled according to the inputs.

In PH/EN and PWM mode, if after the t_{OFF} time has elapsed but the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration until current drops below I_{TRIP}.

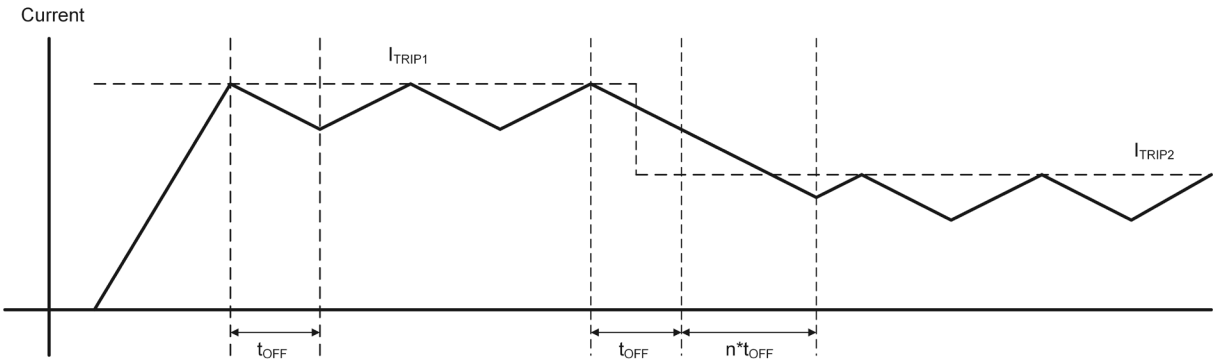


Figure 5.2 Current Regulation in PH/EN and PWM mode

While in independent half bridge mode, if after the t_{OFF} time has elapsed but the current is still higher than the I_{TRIP} level, the device drives t_{BLANK} time then enforces t_{OFF} decay time until current drops below I_{TRIP}.

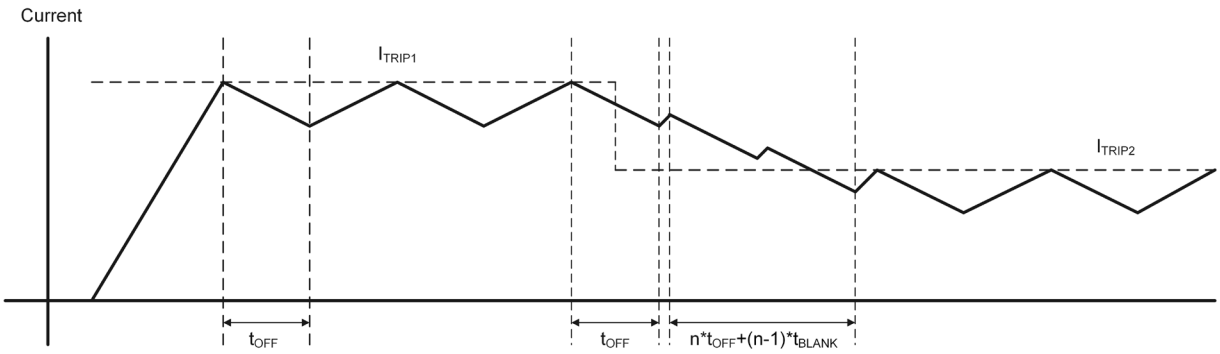


Figure 5.3 Current Regulation in independent half bridge mode

The drive time (t_{DRIVE}) depends heavily on the VM voltage, the back-EMF of the motor, and the inductance of the motor. During the t_{DRIVE} time, the current-sense regulator does not enforce the ITRIP limit until the t_{BLANK} time has elapsed.

6.Open Load Diagnosis

The OLD diagnostic detects if the output terminals (OUT1 and OUT2) are disconnected from the loads to cater to a safer and more robust system. Open load detection works in both standby mode (OLP) and active mode (OLA). OLP detects the presence of the motor prior to commutating the motor. While OLA detects the motor disconnection from the driver during commutation.

6.1.Passive Open Load Diagnosis

The passive OLD, which is also called offline open load diagnostic, is carried out before the FETs are turned on. This diagnostics feature ensures that the load is connected to the driver before driving the load.

Figure 6.1 shows the passive OLD circuit implementation. All of the FETs are in Hi-Z state, while a minimal amount of diagnostic current flows through the load for a short amount of time to test the load's connection to the FETs. The diagnostic current must be very small to avoid load rotation. This internal source / sink diagnostic current drive current into the load connected between OUT1 and OUT2 during a set deglitch time and are limited by the load's resistance. If the load is connected between OUT1 and OUT2, a low-impedance path is created, causing the diagnostics current to be high and operate in saturation. However, if the load is disconnected from the either of OUT1 and OUT2, a high-impedance path is created, causing the current to be reduced to zero. So the voltage at the comparators inputs fluctuates with this diagnosis current variation. When the comparator positive terminals are greater than the negative reference voltage terminals, the comparator outputs are high. These comparator results output the OLD flags.

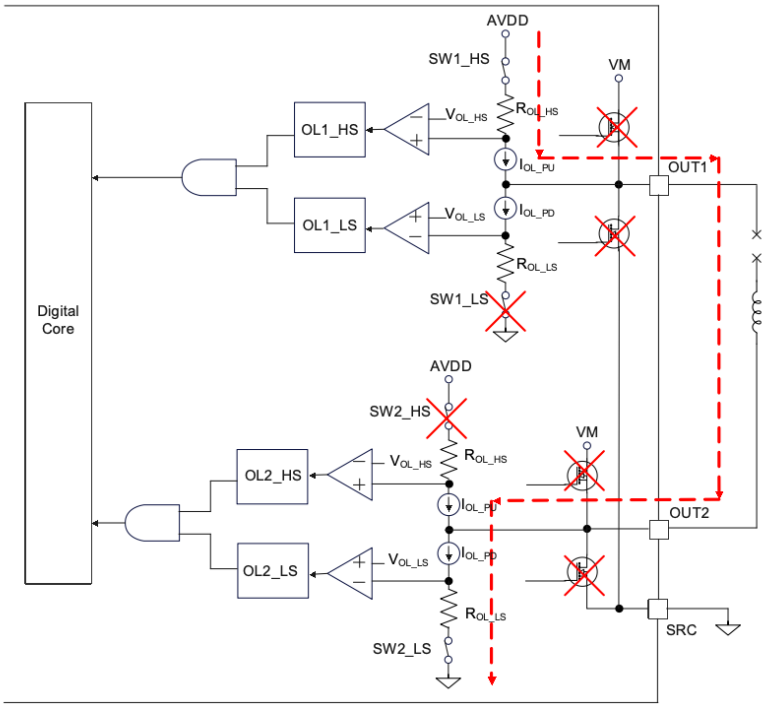


Figure 6.1 Passive Open Load Detection Circuit

For H-bridge application, the passive OLD sequence runs in two steps. First enable the OUT1 pullup current source (turn on SW1_HS) and OUT2 pulldown current source (turn on SW2_LS) for 0.5*td(OL). If a load is connected, the current passes through the pullup resistor and the OLx_HS comparator output remains low. If an OL condition exists, the current through the pullup resistor goes to 0 A which results $V_{OLx\_HS}(+) > V_{OLx\_HS}$ and the OLx_HS comparator trips high. Second enable the OUT1 pulldown current source (turn on SW1_LS) and OUT2 pullup current source (turn on SW2_HS) for the other 0.5*td(OL). In the same way, the OLx_LS comparator output either remains low to indicate that a load is connected, or trips high if $V_{OLx\_LS}(-) < V_{OLx\_LS}$ to indicate an OL condition. Only if both the OLx_HS and OLx_LS comparators report an OL condition, the OUTx is confirmed as open load fault.

6.1.1.Full Bridge application

Below shows how to calculate the minimum open load resistance in full bridge application that can be detected as open load fault.

The OLD monitoring depends on the load resistance (R_L). The load's current (I_L) for a load connected between OUT1 and OUT2 is calculated as,

$$I_L = \frac{AVDD}{R_{OL\_HS} + R_{OL\_LS} + R_L}$$

HS comparator positive input voltage is calculated as,

$$V_{OL\_HS}(+) = AVDD * \frac{R_{OL\_LS} + R_L}{R_{OL\_HS} + R_{OL\_LS} + R_L}$$

LS comparator negative input voltage is calculated as,

$$V_{OL\_LS}(-) = \frac{AVDD}{R_{OL\_HS} + R_{OL\_LS} + R_L} * R_{OL\_LS}$$

Only if $V_{OL\_HS}(+)$ greater than V_{OL_HS} and $V_{OL\_LS}(-)$ less than V_{OL_LS}, the output of OLx_HS and OLx_LS comparators are all set to high. So in order to report OL fault, minimum load resistance R_L should simultaneously satisfy below two formula:

$$R_L > \frac{V_{OL\_HS}(+) * (R_{OL\_HS} + R_{OL\_LS}) - AVDD * R_{OL\_LS}}{AVDD - V_{OL\_HS}(+)}$$
$$R_L > \frac{AVDD * R_{OL\_LS} - V_{OL\_LS}(-) * (R_{OL\_HS} + R_{OL\_LS})}{V_{OL\_LS}(-)}$$

For NSD7315-Q1, AVDD is 5V, V_{OL_HS} is 4V, $V_{OL_LS}(-)$is 1V, R_{OL_LS} and are 1 kΩ. So minimum load resistance R_L should be greater than 3kΩ for OLx_HS and OLx_LS to be set to high, to report OL flag.

6.1.2.Half Bridge and load connect to supply application

NSD7315-Q1 also can be used as half bridge. Below shows how to calculate the minimum open load resistance in half bridge and load connect to supply application that can be detected as open load fault.
The load's current (I_L) for a load connected between OUTx and VM is calculated as,

$$I_L = \frac{VM}{R_{OL\_LS} + R_L}$$

In this case, HS comparator positive input voltage is always larger than V_{OL_HS} no matter R_L value, so the output of OLx_HS comparator is always high.
LS comparator negative input voltage is calculated as,

$$V_{OL\_LS}(-) = \frac{VM}{R_{OL\_LS} + R_L} * R_{OL\_LS}$$

Only if $V_{OL\_HS}(+)$ greater than V_{OL_HS} and $V_{OL\_LS}(-)$ less than V_{OL_LS}, the output of OLx_HS and OLx_LS comparators are all set to high. So in order to report OL fault, minimum load resistance R_L should satisfy below formula:

$$R_L > \frac{(VM - V_{OL\_LS}(-)) * R_{OL\_LS}}{V_{OL\_LS}(-)}$$

For NSD7315-Q1, $V_{OL_LS}(-)$is 1V, R_{OL_LS} is 1 kΩ. Consider VM 13.5V, minimum load resistance R_L should be greater than 12.5kΩ for OLx_HS and OLx_LS to be set to high, to report OL flag.

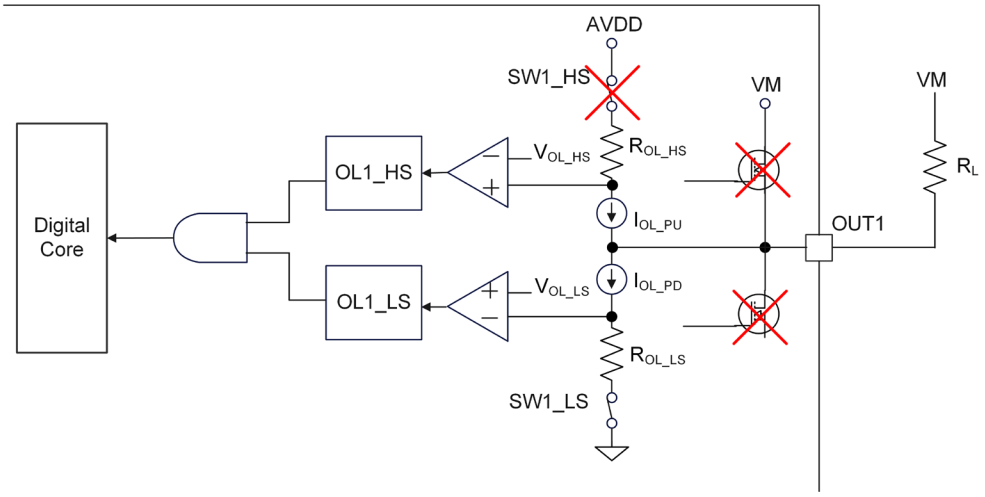


Figure 6.2 Passive OLD for load connected to VM

6.1.3.Half Bridge and load connect to ground application

Below shows how to calculate the minimum open load resistance in half bridge and load connect to ground application that can be detected as open load fault.

The load's current (I_L) for a load connected between OUTx and GND is calculated as,

$$I_L = \frac{AVDD}{R_{OL\_HS} + R_L}$$

In this case, LS comparator negative input voltage is always less than V_{OL_LS} matter R_L value, so the output of OLx_LS comparator is always high.

HS comparator positive input voltage is calculated as,

$$V_{OL\_HS}(+) = \frac{AVDD}{R_{OL\_HS} + R_L} * R_L$$

Only if $V_{OL\_HS}(+)$ greater than V_{OL_HS} and $V_{OL\_LS}(-)$ less than V_{OL_LS}, the output of OLx_HS and OLx_LS comparators are all set to high. So in order to report OL fault, minimum load resistance R_L should satisfy below formula:

$$R_L > \frac{V_{OL\_HS}(+) * R_{OL\_HS}}{(AVDD - V_{OL\_HS}(+))}$$

For NSD7315-Q1, is 5V, $V_{OL\_HS}(+)$ is 4V, R_{OL_HS} is 1 kΩ. So minimum load resistance R_L should be greater than 4kΩ for OLx_HS and OLx_LS to be set to high, to report OL flag.

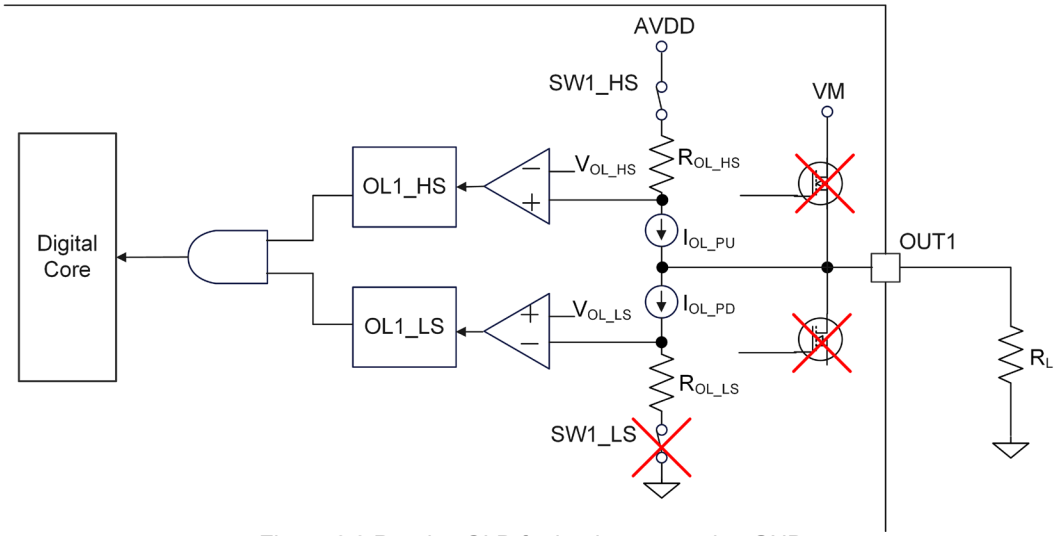


Figure 6.3 Passive OLD for load connected to GND

Table 6.1 is summary for minimum open load resistance in full bridge and half bridge application.

Table 6.1 Resistance for Open Load Detection

Node1	Node2	Resistance	Comments
OUT1	OUT2	3kΩ	
OUTx	VM	13kΩ	V_{VM} = 13.5V
OUTx	GND	4kΩ	

6.1.4.Passive OLD delay time selection

The OLP_DLY bit is used to configure open load diagnostic delay time. This time selection depends on output capacitance value. If output capacitance less than 15nF, OLP_DLY bit is set to 0b, that delay time is 0.3ms. If output capacitance larger than 15nF and less than 60nF, OLP_DLY bit is set to 1b, that delay time is 1.2ms. If output capacitance approximates to 60nF while OLP_DLY bit set to 0b, open load fault can't be reported correctly. Because if there is capacitance on the output pin, once enable OLP function, the diagnostic source/sink current need to charge or discharge the output capacitance through internal OL resistor, which cause comparator input voltage rise/fall has a delay time, so need to configure this delay time correctly before enable OLP function if there is capacitance on the output pin.

6.1.5.Passive OLD sequence

The open load passive diagnostic (OLP) sequence is different for the hardware and SPI version of the device.

For the hardware version of the device, the OLP test is performed only one time after power-up or after exiting sleep mode if the nOL pin is tied to GND. It means that if the device is already powered up or in active mode, then open load fault occurs, the open load fault can't be reported. The OLP test sequence for hardware version is as below:

1.VM power up or nSLEEP turns high.

2.Perform the OLP test before the ton or tWAKE time to expire.
• If an open load (OL) is detected, the nFAULT pin is driven low after td(OL)=0.3ms elapses from internal current sources enabled.

3.Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

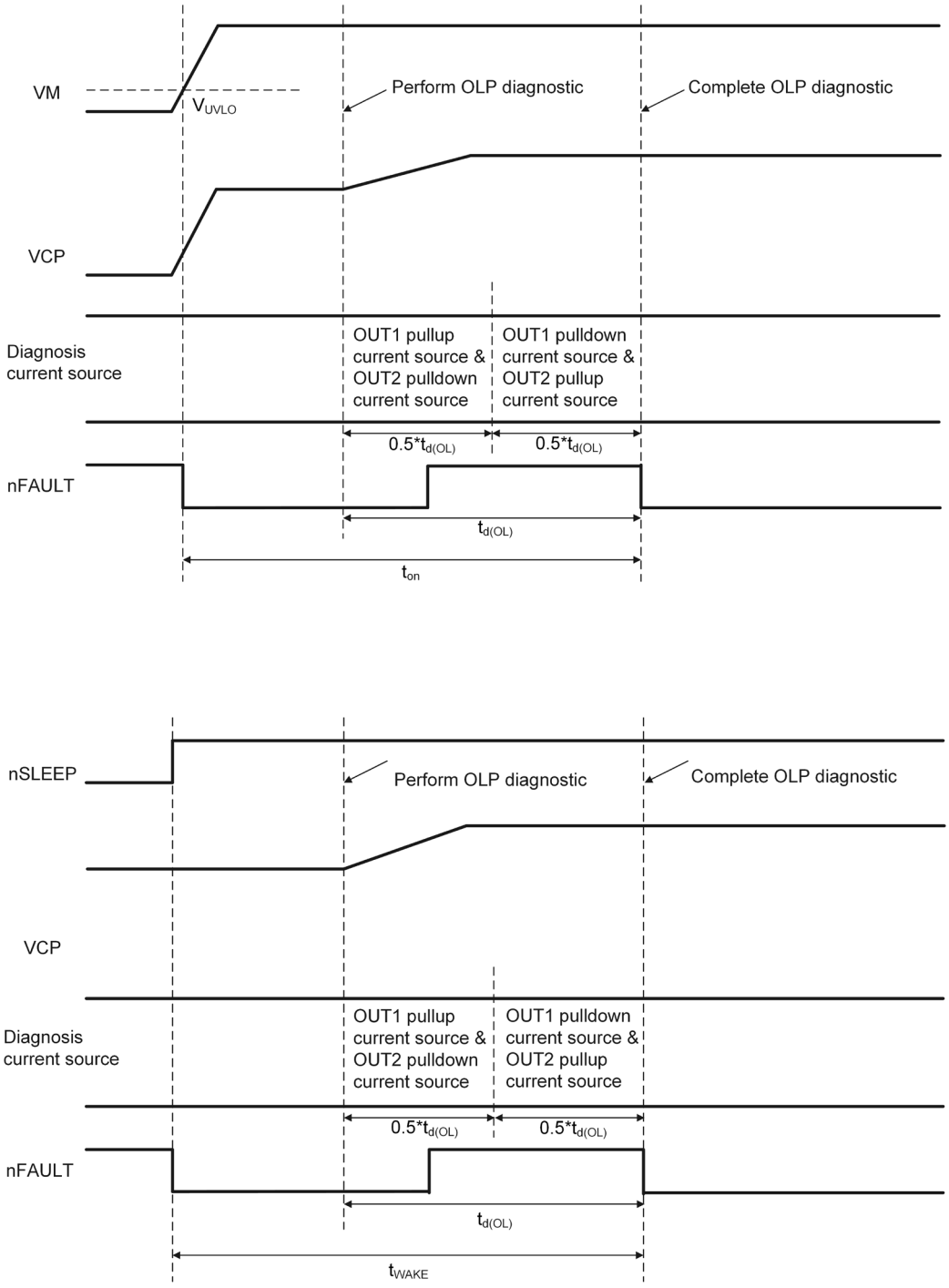


Figure 6.4 OLP sequence of Hardware version

For the SPI version of the device, the OLP test is performed when commanded. It can be performed at any time after power-up or after exiting sleep mode. The OLP test sequence for SPI version is as below:

1.Set the pin DISABLE high (to disable the half bridge outputs).

2.Wait for the $t_{DISABLE}$ time to expire.

3.Write 1b to the EN_OLP bit in the IC1 register.

4.Perform the OLP test.
• If an OL condition is detected, the nFAULT pin is driven low, and the FAULT, OLD and OLx bits are latched high.
• After OLP detection completed, the EN_OLP bit returns to the default setting (0b) after the $t_{d(OL)}$ time expires.

5.Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

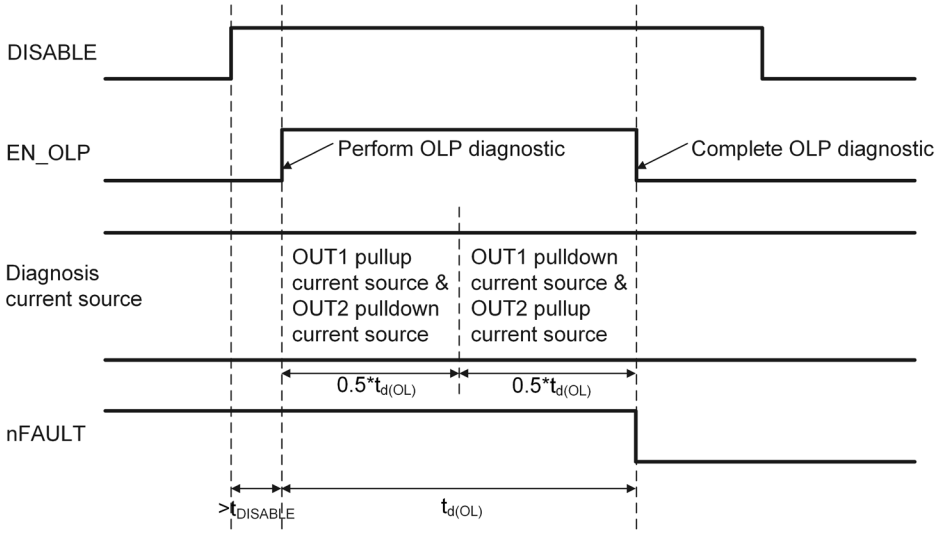


Figure 6.5 OLP sequence of SPI version

The EN_OLP register maintains the written command until the diagnostic is complete. The signal on the DISABLE pin must remain high for the entire duration of the test. While the OLP test is running, if the DISABLE pin goes low, the OLP test is aborted to resume normal operation and no fault is reported. The OLP test is not performed if the motor is energized.

For the SPI version of the device, if perform several times OLP diagnostic through write several times 1b to EN_OLP bit in the IC1 register, the last diagnostic result will overwrite the former diagnostic results. For example, if open load condition exists, after write 1b to EN_OLP bit, the nFAULT pin and FAULT, OLD and OLx bits report OL fault. Then if open load condition is removed, after write 1b to EN_OLP bit again, nFAULT is released and FAULT, OLD and OLx bits are reset.

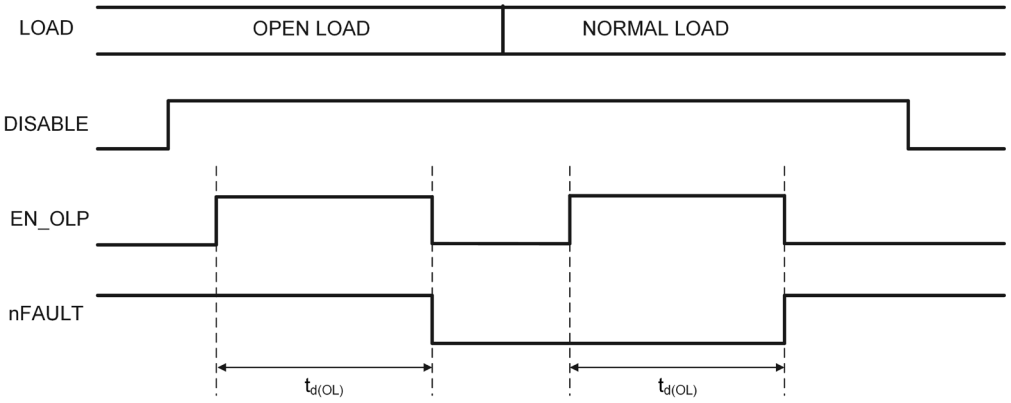


Figure 6.6 Several times OLP diagnostic

6.2.Active Open Load Diagnosis

The active OLD, which is also called online OLD, is carried out while the FETs driving the load are turned on. Active OLD ensures that the load is connected to the driver during the operation. While the load is in operation, the current flowing through the FETs is monitored to ensure that the load is connected.

The active OLD is based on the voltage in a high-side FET's body diode during the current re-circulation. The current re-circulation occurs through the high-side FET's body diode in asynchronous rectification. Figure 6.7 shows the flow of current during forward drive and during current re-circulation. The high-side FET of OUT1 is in operating state. The voltage across the body diode of the current re-circulation high-side FET is compared with the fixed OLA threshold voltage (V_{OLA}) to detect the OLD event. An OLD occurs when the voltage drop across the body diode of the current re-circulation FET does not exhibit overshoot greater than the V_{OLA} over VM during the current-re-circulation time. An OLD does not occur if the energy stored in the load is high enough to cause an overshoot greater than the V_{OLA} over VM. The overshoot is caused by the current flowing through the body diode of the current re-circulation FET.

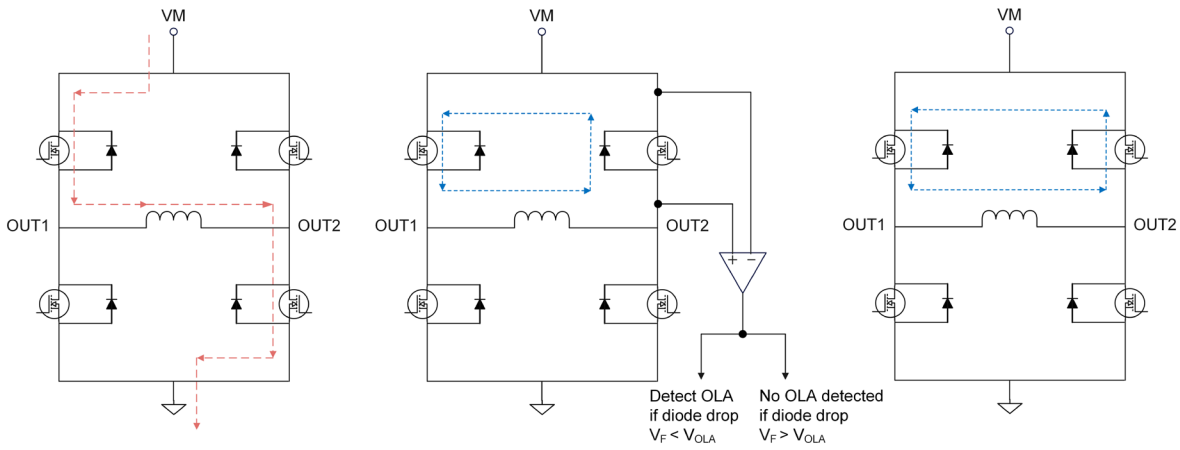


Figure 6.7 Active Open Load Detection Circuit

To avoid inadvertently triggering the open load diagnosis, a failure counter is implemented. Three consecutive occurrences of the internal open-load signal must occur, essentially three consecutive PWM pulses without freewheeling detected, before an open load condition is reported by the nFAULT pin and in the respective SPI register.

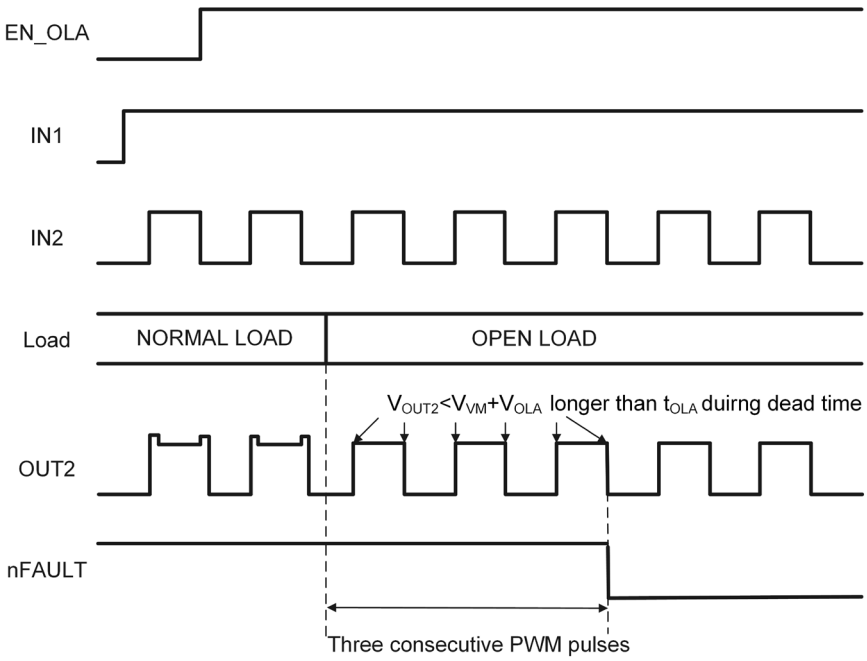


Figure 6.8 OLA sequence for SPI version

In PH/EN and PWM mode, the motor current decays only by high-side recirculation. In independent half bridge mode, the motor current can decay by high-side recirculation, also can decay by low-side recirculation. If using low-side recirculation, the diode VF voltage of high-side FET is always less than the VOLA voltage, so an open load fault is reported even though the load is normally connected across output pins. In this case, the OLA mode should not be used. Also for half bridge and load connect to ground application, will result in false trips of the active open load diagnosis (OLA).

Table 6.2 OLA for different configuration

Control Mode	Load Connection		Decay Mode	OLA
PH/EN	Full-Bridge		High-side	Operational
PWM	Full-Bridge		High-side	Operational
Independent half bridge	Full-Bridge		High-side	Operational
	Full-Bridge		Low-side	Not Available
	OUTx	GND	Low-side	Not Available
	OUTx	VM	High-side	Operational

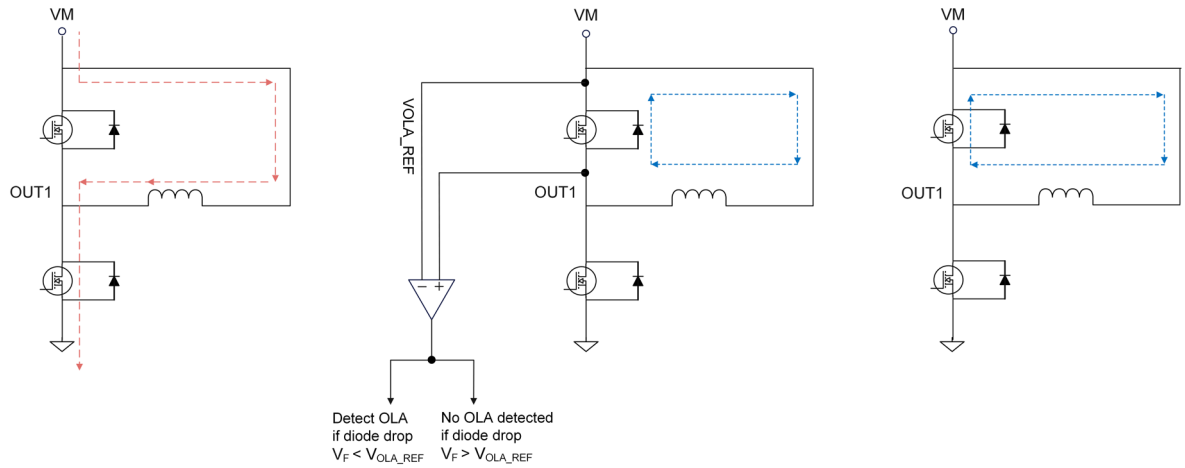


Figure 6.9 High-side recirculation in Independent half bridge mode

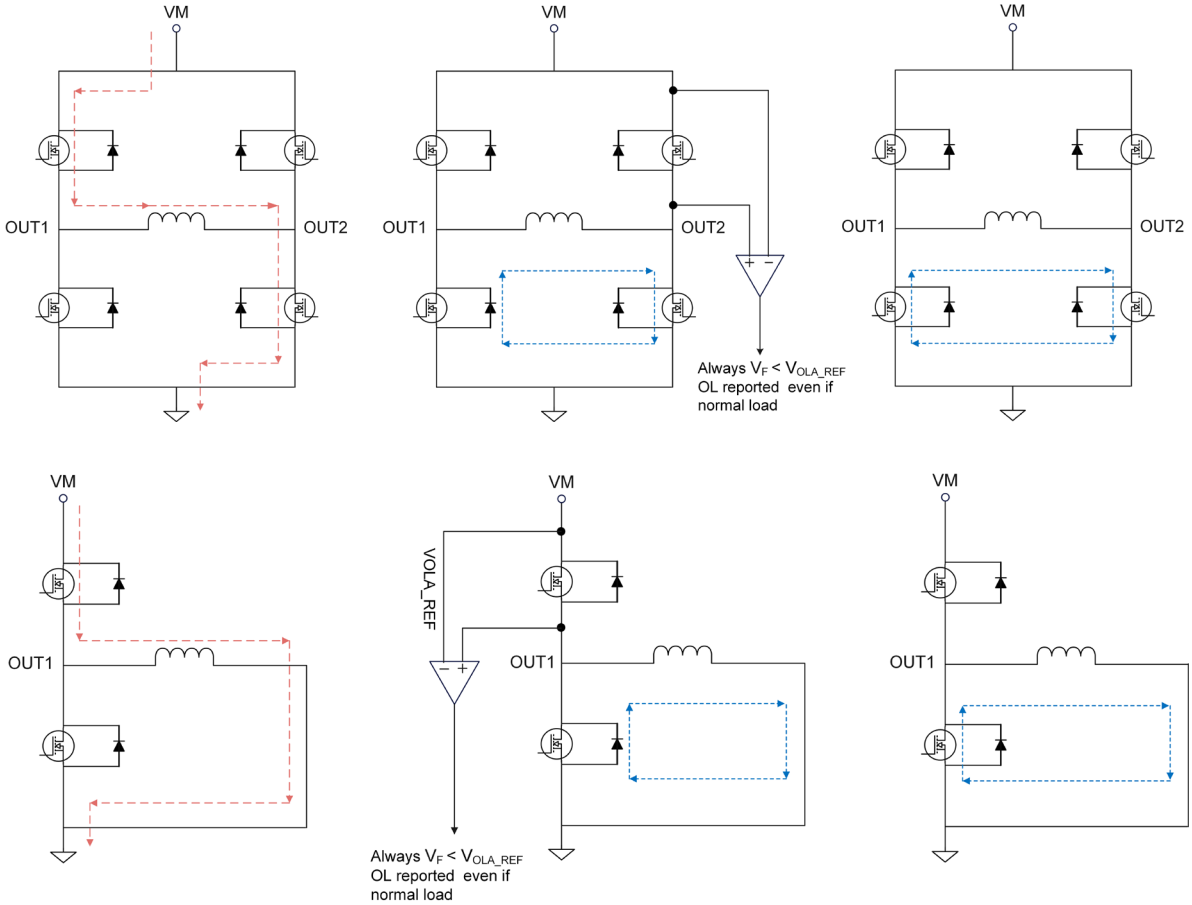


Figure 6.10 Low-side recirculation in Independent half bridge mode

Note: Depending on the operation conditions and external circuitry, such as the output capacitors, an open load condition could be indicated even though the load is present. This case might occur, for example, during a direction change or for small load currents with respectively small PWM duty cycles. Therefore, recommend that evaluating the open load diagnosis only in known, suitable operating conditions and to ignore it otherwise.

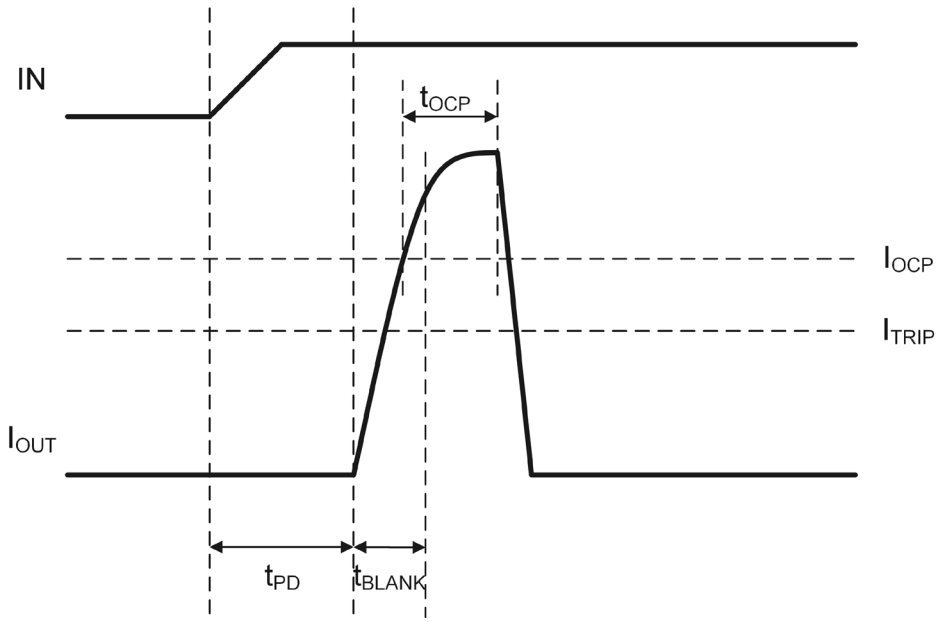
7.Overcurrent Protection

If the battery voltage is low and short inductance is a little big (short wire is long), it may cause ITRIP regulation to trigger ahead of the OCP detection, resulting in the device missing the short detection. When load current reaches higher than I_{TRIP} value, in order to determine the device to enter overcurrent mode or current regulation mode, below scenario is enforced.

In short occurs ahead of channel on case, if current rise to I_{OCP} before t_{BLANK} expire, the device enters overcurrent mode. OCP fault will be reported after current higher than I_{OCP} for t_{OCP}.

In channel on ahead of short occurs case, if current rise to I_{OCP} before t_{DEG} expire, the device enters overcurrent mode. OCP fault will be reported after current higher than I_{OCP} for t_{OCP}.

In channel on ahead of short occurs case, if current doesn't rise to I_{OCP} when t_{DEG} expire, the device enters current regulation mode (not report OCP). When current reaches I_{TRIP} and last for t_{DEG}, the device enforces slow current decay.



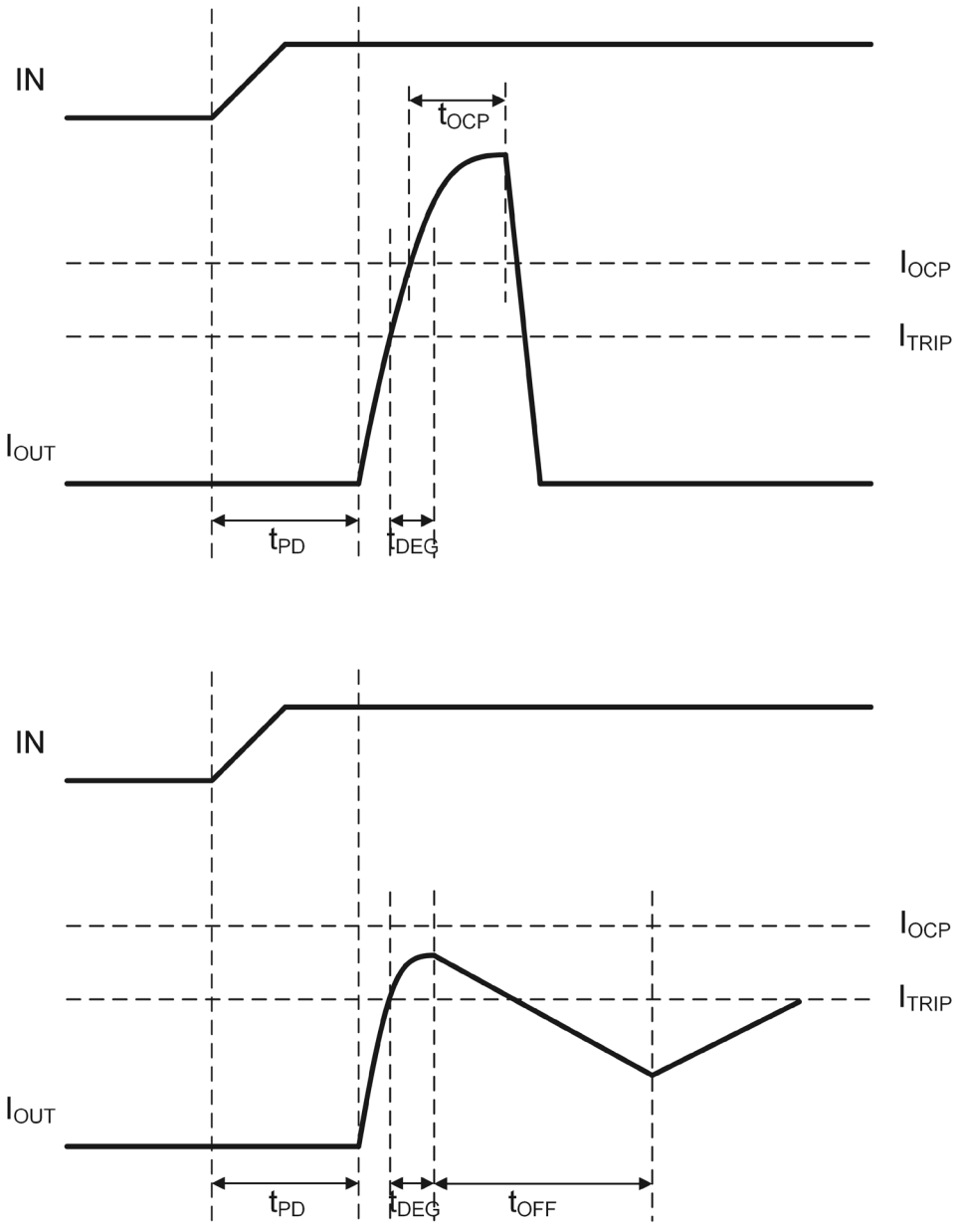


Figure 7.1 OCP scenario

8.Fault Response

Table 8.1 Fault Response

Fault	Condition	Configuration	Report	Half Bridge	Logic	Recovery
VM undervoltage (UVLO)	V_{VM} < V_{UVLO} (maximum 4.45V)	-	nFAULT FAULT, UVLO bit	Hi-Z	Active	Automatic: V_{VM} > V_{UVLO} (maximum 4.7V); UVLO bit remains set until CLR_FLT/ nSLEEP
VM UVLO reset	V_{VM} < V_{RST} (maximum 4.1V)	-	Disable	Hi-Z	Reset	Automatic: V_{VM} > V_{UVLO}
Charge pump undervoltage (CPUV)	V_{VCP} < $V_{VCP(UV)}$ (typical V_{VM}+2.3V)	DIS_CPUV = 0b	nFAULT FAULT, CPUV bit	Hi-Z	Active	Automatic: V_{VCP} > $V_{VCP(UV)}$ (typical V_{VM} + 3.5V); CPUV bit remains set until CLR_FLT/ nSLEEP
		DIS_CPUV = 1b	None	Active	Active	No Action
Overcurrent (OCP)	I_O > I_{OCP} (minimum 10A)	OCP_MODE = 00b	nFAULT FAULT, OCP, OCP_xx bit	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		OCP_MODE = 01b	nFAULT FAULT, OCP, OCP_xx bit	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT FAULT, OCP, OCP_xx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		OCP_MODE = 11b	None	Active	Active	No Action
Overcurrent (OCP)	No load detected	EN_OLP = 1b	nFAULT FAULT, OLD, OLx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		EN_OLA = 1b	nFAULT FAULT, OLD, OLx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
Current regulation (ITRIP)	I_O > I_{TRIP_LVL}	ITRIP_REP = 0b	ITRIPx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
		ITRIP_REP = 1b	nFAULT FAULT, ITRIPx bit	Active	Active	Reporting Latched: CLR_FLT/ nSLEEP
Thermal shutdown (TSD)	T_J > T_{TSD} (minimum 165°C)	TSD_MODE = 0b	nFAULT FAULT, TSD bit	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		TSD_MODE = 1b	nFAULT FAULT, TSD bit	Hi-Z	Active	Automatic: T_J < T_{TSD} - T_{HYS} TSD bit remains set until CLR_FLT/ nSLEEP
Thermal Warning (OTW)	T_J > T_{OTW} (minimum 140°C)	OTW_REP = 0b	OTW bit	Active	Active	Automatic: T_J < T_{OTW} - T_{HYS}
		OTW_REP = 1b	nFAULT FAULT, OTW bit	Active	Active	Automatic: T_J < T_{OTW} - T_{HYS}

9.Hardware version

The following configuration settings are fixed for the hardware version:

- CPUV is enabled
- OCP_MODE is latched shutdown
- TSD_MODE is automatic recovery
- OLP_DLY is 300μs
- OLP and OLA is activated when the open load diagnostic is enabled by the nOL pin (nOL pin is tied to GND)
- ITRIP level is 6.5A if current regulation is enabled by the nITRIP pin (nTRIP pin is open or tied to GND)
- TOFF is 40us
- ITRIP not trigger nFAULT
- OTW not trigger nFAULT
- Control Mode setting is determined by MODE pin connection
- Slew rate setting is determined by SR pin connection/resistor
- No option to independently set the outputs (OUTx) to the Hi-Z state
- nSLEEP low pulse(suggest 10μs) to clear faults
- nSLEEP low pulse(suggest higher than 50μs) will shut down device

10.Power up and down sequence

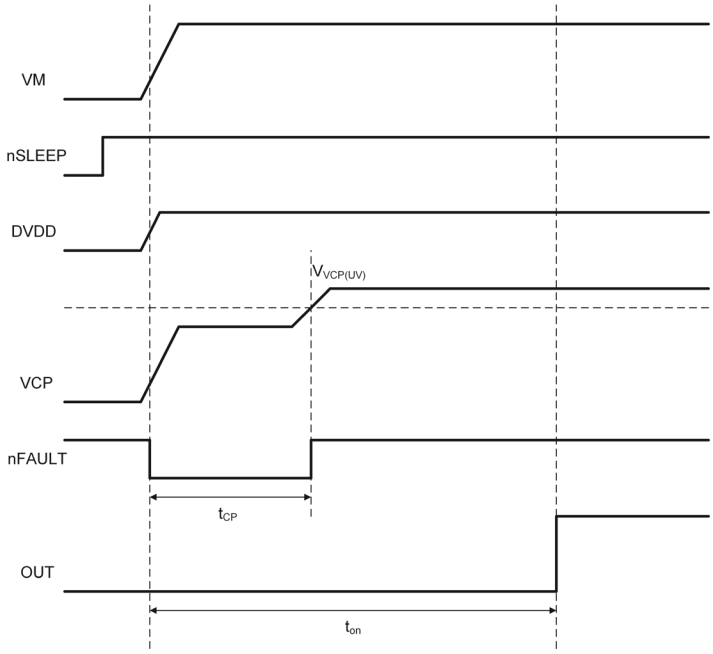


Figure 10.1 Fast power up sequence

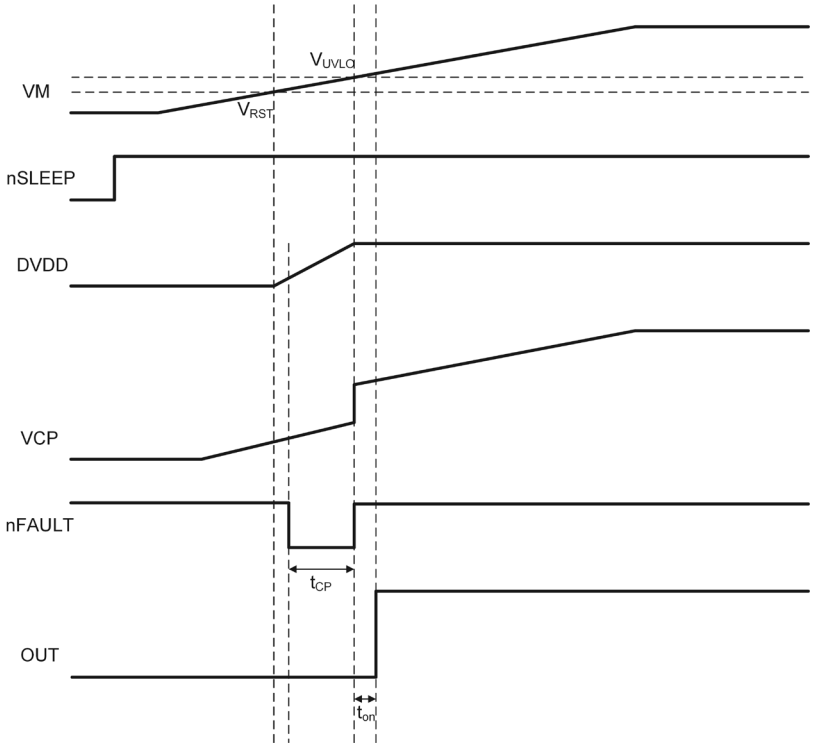


Figure 10.2 Slow power up sequence

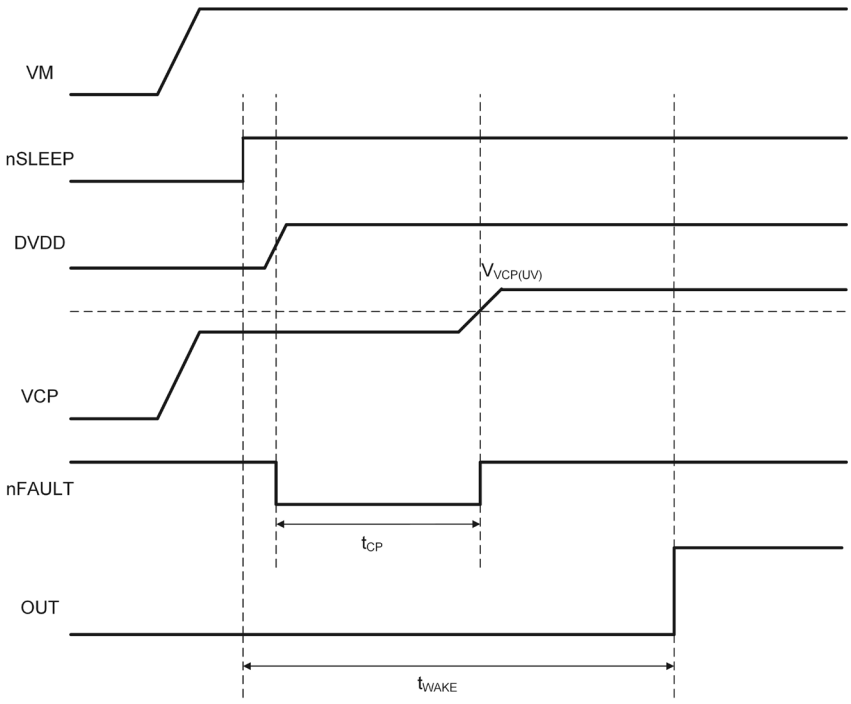


Figure 10.3 Exit sleep mode sequence

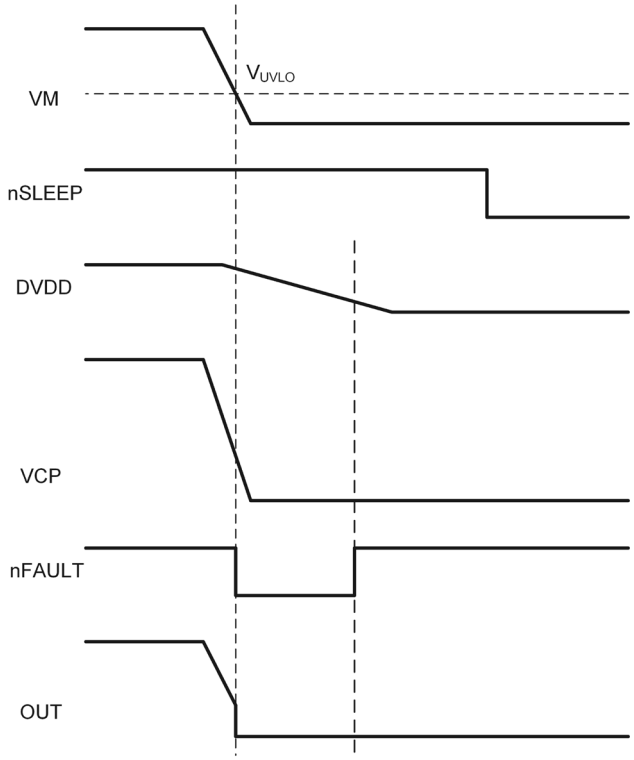


Figure 10.4 Power down sequence

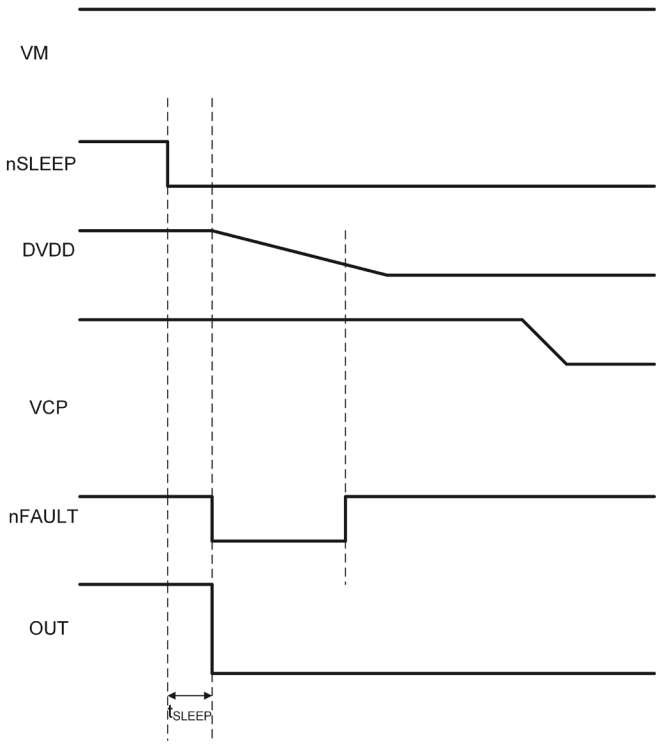


Figure 10.5 Enter sleep mode sequence

11.Application Information

Figure 11.1 and 11.2 show the typical application schematic for the SPI version and HW version of the device.

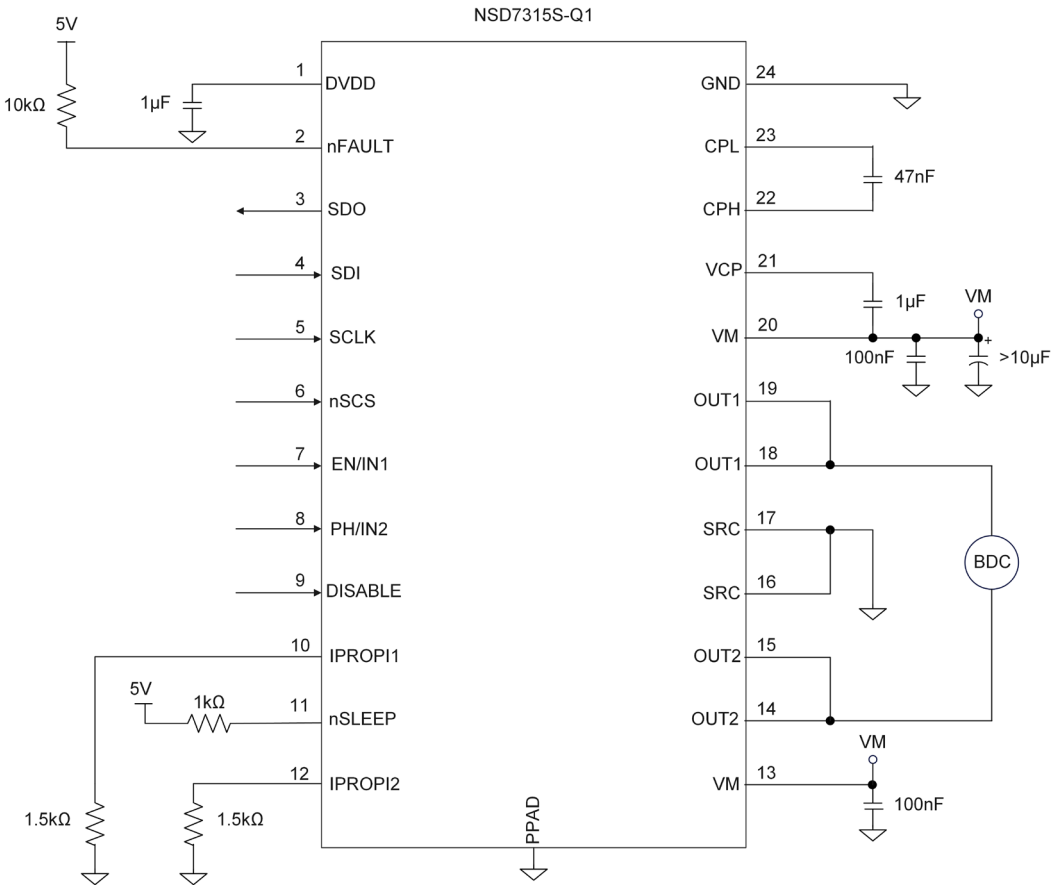


Figure 11.1 Typical application schematic of SPI version

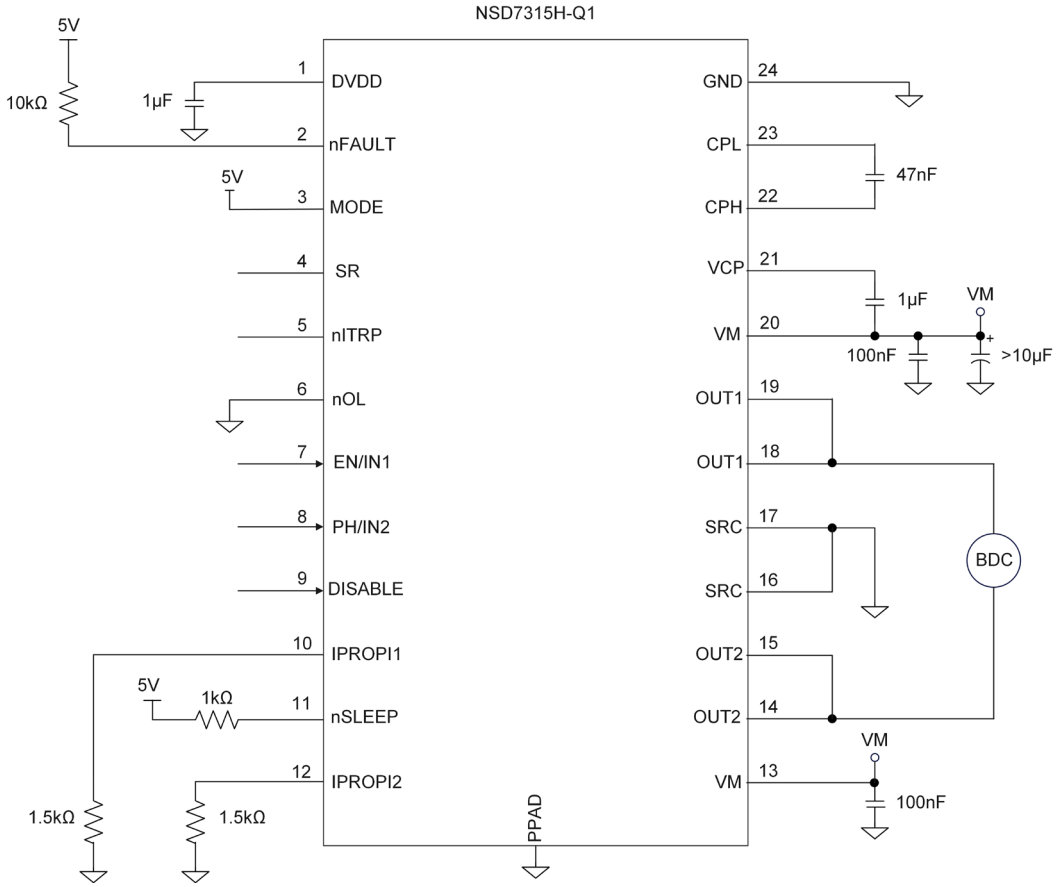


Figure 11.2 Typical application schematic of HW version

Table 11.1 lists the recommended external components for the device.

Table 11.1 External Components

Component	PIN1	PIN2	Recommended
C_{VM1}	VM	GND	100nF ceramic capacitor rated for VM
C_{VM2}	VM	GND	Bulk capacitor rated for VM
C_{VCP}	VCP	VM	16V, 1μF ceramic capacitor
C_{FLY}	CPH	CPL	47nF capacitor rated for VM
C_{DVDD}	DVDD	GND	6.3V, 1μF ceramic capacitor
R_{nFAULT}	5V	nFAULT	≧10kΩ pullup resistor to external 5V supply
*R_{nSLEEP}	5V	nSLEEP	≦1kΩ series resistor to external 5V supply
$R_{SENSE-1}$	IPROPI1	GND	Resistors to convert mirrored current into a voltage
$R_{SENSE-2}$	IPROPI2	GND	Resistors to convert mirrored current into a voltage

*Note: The series resistor on nSLEEP pin (R_{nSLEEP}) should be lower than 1kΩ.

12.Power Dissipation Calculation

Total power dissipation for the device is composed of three main components. These are the supply current dissipation, the power MOSFET switching losses, and the power MOSFET $R_{DS(ON)}$ (conduction) losses.

$$P_{TOT} = P_{VM} + P_D + P_{SW}$$

P_{VM} can be calculated from the nominal supply voltage (V_M) and the supply current (I_{VM}) in active mode.

$$P_{VM} = V_M \times I_{VM}$$

P_D can be calculated from the RMS current (I_{RMS}) and the power MOSFET $R_{DS(ON)}$.

$$P_D = I_{RMS}^2 \times (R_{DS(on)High\text{-}side} + R_{DS(on)Low\text{-}side})$$

P_{SW} can be calculated from the nominal supply voltage (V_M), average output current (I_{RMS}), switching frequency (fPWM) and the device output rise and fall times (t_{SR}) time specifications.

$$P_{SW} = P_{SW\_RISE} + P_{SW\_FALL} = 0.5 \times V_M \times I_{RMS} \times (t_{SR\_RISE} + t_{SR\_FALL}) \times f_{PWM}$$

P_{TOT} makes the junction temperature (T_J) of the device to be

$$T_J = T_A + P_{TOT} \times R_{\theta JA}$$

The amount of current the device can drive depends on the power dissipation without going into thermal shutdown.

13.Revision History

Revision	Description	Author	Date
1.0	Initial version	Wenyuan Pi	2026/1/30

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